

AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. APPLICATION NO. 10/627,632
ATTORNEY DOCKET NO. Q76734

REMARKS

Applicant thanks the Patent Office for acknowledging Applicant's claim to foreign priority, and for indicating that the certified copy of the priority document was made of record in U.S. Appln. No. 09/330,162.

Applicant requests that the Patent Office consider the references listed on the PTO/SB/08 A & B form submitted with the Information Disclosure Statement filed on July 28, 2003 and return an initialed copy of the PTO/SB/08 A & B, thereby confirming that the listed references have been considered.

The Patent Office objects to the Drawings under 37 C.F.R. § 1.83(a) as not including every feature of the invention. Specifically, the Patent Office asserts that the recitation of "a stage of converting terminal voltage of the capacitor to a logic signal and outputting the logic signal" is not shown in the Drawings. Applicant submits that the Patent Office is overlooking the threshold buffer-capacitor arrangement shown in Figure 5(a) and Figure 6, and described at page 22, lines 1-4 of the instant specification. Thus, Applicant respectfully submits that the objection to the Drawings is moot, and respectfully requests that the objection be withdrawn.

The Patent Office objects to the disclosure under 37 C.F.R. § 1.71 as allegedly being incomprehensible. Specifically, the Patent Office claims that a stage that converts a capacitor's terminal voltage into a logic signal is not understood. Applicant points to page 22, lines 1-4 of the disclosure as containing the text that describes the threshold buffer-capacitor arrangement, *i.e.*, the conversion of a capacitor's terminal voltage into a logic signal. Thus, Applicant

respectfully submits that the objection to the disclosure is moot, and respectfully requests that the objection be withdrawn.

Claim 7 has been examined on its merits, and is the only claim presently pending in the application.

1. Claim 7 stands rejected under 35 U.S.C. § 112 (2nd para.) as allegedly being indefinite. Applicant traverses the rejection of claim 7 for at least the reasons discussed below.

The Patent Office asserts that it is unclear how the recitation of “a stage of converting terminal voltage of the capacitor to a logic signal and outputting the logic signal” reads on the preferred embodiment. As noted above with respect to the 37 C.F.R. § 1.71 objection to the disclosure, the text at page 22, lines 1-4 describes the threshold buffer-capacitor arrangement, *i.e.*, the conversion of a capacitor’s terminal voltage into a logic signal. Furthermore, Figures 5(a) and 6 depict the threshold buffer-capacitor arrangement that converts terminal voltage of the capacitor to a logic signal.

The Patent Office further alleges that claim 7 reads on Figures 3, 5(a), 5(b) and 20. Claim 7 recites, *inter alia*, “a stage of varying the charging or discharging speed of the capacitor by shifting switching control timings of switches in said switch group.” Figures 3, 5(a), 5(b) or 20 depict the “stage of varying” as recited in claim 7. However, the delay circuits (DL1, DL2) depicted in Figure 6 and the phase shift circuit (1001) depicted in Figure 12 would fulfill this recitation of claim 7.

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Thus, Applicant submits that the 35 U.S.C. § 112 (2nd para.) rejection of claim 7 has been overcome, and respectfully requests withdrawal of same.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

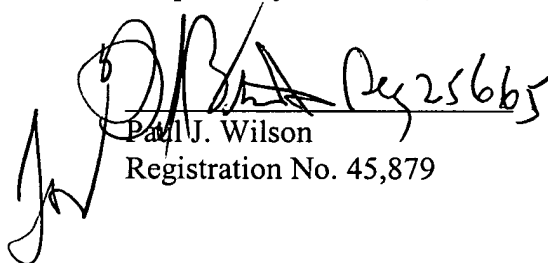
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